What is claimed is:

1. An apparatus for performing message passing decoding operations, the apparatus comprising:

memory including a set of memory locations for storing L sets of Z K-bit messages, where Z is a positive integer greater than one and K and L are non-zero positive integers;

a node processor including a plurality of node processing units, each node processing unit for performing at least one of a constraint node processing operation and a variable node processing operation; and

a switching device coupled to the memory and to the node processing unit, the switching device for passing sets of Z K-bit messages between said memory and said node processor and for reordering the messages in at least one of said sets of messages in response to switch control information.

2. The apparatus of claim 1, further comprising:

a message ordering control module coupled to said switching device for generating said switch control information used to control the reordering of messages in said at least one set of messages.

3. The apparatus of claim 2, wherein the switching device includes circuitry for performing a message rotation operation to reorder messages included in a set of messages.

4. The apparatus of claim 2, wherein the message ordering control module stores information on the order

sets of messages are to be read out of the memory and information indicating what reordering of messages is to be performed by said switch on individual sets of messages read out of the memory.

5. The apparatus of claim 2, wherein the message ordering control module is further coupled to said memory and sequentially generates set identifiers, each set identifier controlling the memory to access memory locations corresponding to a set of messages as part of a single read or write operation.

6. The apparatus of claim 5, wherein each set identifier is a single memory address.

7. The apparatus of claim 2, wherein said plurality of node processing units includes Z node processing units arranged in parallel, each one of the Z node processing units operating in parallel to process a different message in each set of Z messages passed between said memory and said node processor.

8. The apparatus of claim 7, wherein said memory includes an address input which allows each set of messages to be addressed as a unit thereby enabling a set of messages to be read from said memory in a single SIMD read operation.

9. The apparatus of claim 7, wherein said memory includes an address input which allows each set of

messages to be addressed as a unit thereby enabling a set of messages to be written into said memory in a single SIMD write operation.

10. The apparatus of claim 1, wherein each of said plurality of node processing units includes a control signal input for receiving a control signal to switch node processing unit operation between a constraint node mode of processing operation and a variable node mode of processing operation.

11. The apparatus of claim 10, further comprising:

a decoder control device coupled to said plurality of node processing units, the decoder control device generating said control signal used to control said plurality of node processing units.

12. The apparatus of claim 11, wherein each of the Z processing units performs a variable node low density parity check message processing operation to generate at least one new message from at least one message received from said switching device.

13. The apparatus of claim 10,

wherein at least one of the plurality of node processing units includes information indicating a number of messages to be used in each of a plurality of sequential variable node processing operations.

14. The apparatus of claim 7,

wherein the decoder control device is further coupled to said message passing control device; and

wherein the message passing control device specifies a different order in which each of the L sets of Z messages are to be read out of the memory during the variable node mode of processing operation than during constraint node mode of processing operation.

15. The apparatus of claim 2, further comprising a decoder control module coupled to the message ordering module, the decoder control module including means for supplying information to the message ordering module used to control the order in which each of the L sets of Z messages are to be read out of said memory.

16. The apparatus of claim 15, wherein the decoder control device further includes means for supplying an edge index to the message ordering module which controls the generation of the set identifiers supplied to said memory.

17. The apparatus of claim 16, further comprising a degree memory coupled to the node processor for storing a set of node degree information.

18. The apparatus of claim 17, wherein the control device further generates a node index used to determine which node degree information in the stored set of node

degree information is to be supplied to the node processor at any given time.

19. The apparatus of claim 1, further comprising:

a second node processor coupled to said memory, the second node processor including a second plurality of node processing units, each of the second plurality of node processing units for performing at least one of a constraint node processing operation and a variable node processing operation.

20. The apparatus of claim 19, further comprising:

additional memory coupling said node processor to said second node processor, the additional memory including an additional set of memory locations for storing L sets of Z K-bit messages.

21. The apparatus of claim 20, further comprising:

a second switching device coupling said node processor to said additional memory, the second switching device for passing sets of Z K-bit messages between said node processor and said additional memory and for reordering the messages in at least one of the sets of messages passed by the second switch.

22. The apparatus of claim 21,

wherein said node processor is a variable node processor for performing variable node decoder parity check processing operations;

wherein said additional node processor is a constraint node processor for performing constraint node parity check decoder processing operations.

23. The apparatus of claim 21, further comprising:

a parity check verifier, coupled to said additional node processor, for determining from an output of each of the second plurality of processing units included therein, when a parity check decoding operation has been successfully completed.

24. An apparatus for performing message passing decoding operations, the apparatus comprising:

first memory including a first set of memory locations for storing L sets of Z K-bit messages, where L and Z are positive integers greater than one and K is a non-zero positive integer;

a first node processor including a first plurality of node processing units, each node processing unit for receiving at least one K-bit message in each set of Z K-bit messages supplied to the first node processor; and

a first switching device coupling the first memory to the first node processor, the first switching device for passing sets of messages between the first node processor and the first memory and for reordering the messages in at least some of the sets of messages being passed by said first switch.

25. The apparatus of claim 24, further comprising:

a second memory coupled to said first node processor including a second set of memory locations for storing L sets of Z K-bit messages; and

a second node processor coupled to said second memory and to said first memory, the second node processor including a second plurality of node processing units.

26. The apparatus of claim 25, further comprising:

an additional switching device coupling the additional memory to the second node processor, the additional switching device for receiving sets of Z K-bit messages from said additional memory device and for supplying one message in each received set of Z messages to one of said second plurality of node processing units.

27. The apparatus of claim 24, wherein the first node processor is a variable node processor, the apparatus further comprising:

means, coupled to said plurality of processing units included in said first node processor, for determining from an output of each of said first plurality of node processing units when a decoding operation has been successfully completed.

28. A method of performing message passing decoding processing comprising the steps of:

storing L sets of k-bit messages in a memory, each set of K-bit messages including first though Z messages, where L and Z are positive integers greater than one and K is a non-zero positive integer;

reading one of said sets of K-bit messages from memory;

performing a message reordering operation on said read set of K-bit messages to produce a reordered set of Z K-bit messages;

supplying, in parallel, the Z messages in the reordered set of messages to a vector processor; and

operating the vector processor to perform message passing decoder operations using the Z supplied messages as input.

29. The method of claim 26, wherein said message passing decoder operations generate a set of Z decoder messages from the Z messages in the supplied reordered set of messages.

30. The method of claim 29, wherein the step of operating the vector processor to generate Z decoder messages, includes the step of:

performing, in parallel, Z node processing operations.

31. The method of claim 30, wherein each of the Z node processing operations is one of a constraint node processing operation and a variable node processing operation.

32. The method of claim 28, further comprising:

generating a message set identifier indicating the set of Z messages to be read out of memory.

33. The method of claim 32, wherein the step of reading one of said sets of K-bit messages includes:

performing a SIMD read operation using said message set identifier to identify the set of messages to be read from memory.

34. The method of claim 28, further comprising:

performing a second message reordering operation, the second message reordering operation being performed on the generated set of Z decoder messages to produce a reordered set of generated decoder messages.

35. The method of claim 34, further comprising:

storing the reordered set of generated decoder messages in said memory.

36. The method of claim 35, wherein the step of storing the reordered set of generated decoder messages includes performing a SIMD write operation to write said reordered set of generated decoder messages into memory.

37. The method of claim 34, wherein the step of performing a second message reordering operation includes performing the inverse of the message reordering

operation performed on said set of K-bit messages read from the memory.

38. The method of claim 28, further comprising:

accessing stored message set permutation information; and

wherein the step of performing a message reordering operation includes the step of:

performing said reordering as a function of the accessed stored message set permutation information.

39. The method of claim 37, wherein said message set permutation information includes cyclic rotation information.

40. The method of claim 28,

wherein said message passing decoder operations are variable node processing operations, each variable node processing operation including generating a decision value, and

wherein the method further comprises:

examining decision values generated by operating the vector processor to determine if a decoding condition has been satisfied.

41. A method of performing message passing decoding processing, the method comprising the steps of:

operating a node vector processor to generate a set of Z K-bit messages, where L and Z are positive integers greater than one and K is a non-zero positive integer;

performing a message reordering operation on the generated set of Z K-bit messages to produce a reordered set of Z K-bit messages;

performing a single write operation to store the reordered set of z K-bit messages in a memory device.

42. The method of claim 41, wherein the step of performing a single write operation includes performing a SIMD write operation to write the Z messages in the reordered set of messages into memory in parallel.

43. The method of claim 41, wherein the step of operating the node vector processor to generate a set of Z K-bit messages, includes the step of:

performing, in parallel, Z node processing operations, each node processing operation generating one message in said set of Z K-bit messages.

44. The method of claim 43, wherein the Z node processing operations are variable node processing operations.

45. The method of claim 43, wherein the Z node processing operations are constraint node processing operations.

46. The method of claim 43, wherein performing a message reordering operation on the generated set of Z K-bit messages includes:

rotating the messages in the set of Z K-bit messages by performing a switching operation to reorder the messages in the set of messages.

47. A method of performing low density parity check decoder operations, the method comprising:

performing a SIMD read operation to read a stored set of messages;

performing a message reordering operation on the stored set of messages;

supplying the reordered set of messages to node processor including a plurality node processing units arranged in parallel; and

operating the plurality of node processing units to generate a set of updated messages as a function of the supplied reordered set of messages.

48. The method of claim 47, further comprising the step of:

writing the updated messages in said set of updated messages into a memory device using a SIMD write operation.

49. The method of claim 48, further comprising the step of:

performing a message reordering operation on the updated messages in said set of updated messages

prior to writing the updated messages into the memory device.